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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Applicant :	Pervez Hassan Sagarwala	Docket No :	93-C-91D1
Serial No :	09/800,039	Group No :	2822
Filed :	March 6, 2001	Examiner :	Mark V. Prenty
For :	CMOS Integrated Circuit Device With LDD N-Channel Transistor And Non-LDD P-Channel Transistor	Confirmation No :	7946

TRANSMITTAL LETTER

Mail Stop Issue Fee
Attention: Official Draftsman
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice of Allowability (PTO-37) mailed February 27, 2004, for the above-identified patent application, please find enclosed for filing four (4) sheets of formal drawings.

The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account No. 19-1353. A duplicate copy of this sheet is enclosed.

Respectfully submitted

Mario J. Donato, Jr.
Reg. No. 37,816
Attorney for Applicant

STMicroelectronics, Inc.
1310 Electronics Drive/MS 2346
Carrollton, TX 75006
972-466-7503

CERTIFICATE OF MAILING
37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage, in an enveloped addressed to: Mail Stop Issue Fee Attention: Official Draftsman Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-14501 on the date below:

May 10, 2004
Date

Angie Rodriguez
Signature